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EXAMINER	
KUNZER, BRIAN	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,819	LEE, SUK HUN	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-18,20-28 and 30-37* is/are pending in the application.

4a) Of the above claim(s) *27,28 and 30-33* is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,12,16,17,22,23,36 and 37* is/are allowed.

6)☒ Claim(s) *1-3,5,6,9-11,13-15,18,20,21,24-26,34,35,38 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendments

Applicant's amendment in the reply filed on April 13th, 2006 has been received and entered. In summary, claims 4, 19, and 29 have been cancelled, claims 1, 7-10, 12, 13, 15-18, 22-25, 27, 34, and 36-39 have been amended, and claims 27-33 have previously been withdrawn, with only claims 1-3, 5-18, 20-26, and 34-39 pending examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) in view of Yamada (US Patent No. 6,608,330), Emerson (US Patent No. 6,958,497), and Koike (US Patent No. 6,830,948).

With respect to claim 1, Nagahama teaches, from fig. 9 (and columns 34-40), a nitride based 3-5 group compound semiconductor light emitting device comprising:

a substrate (301);

a buffer layer (304) formed above the substrate (301);

a first In doped GaN layer (312) formed above the buffer layer (304);

a super lattice structure layer (313) formed above the first In-doped GaN layer (312);

a first electrode contact layer (311);

an active layer (315) formed above the first electrode contact layer (311) and functioning to emit light;

a second In doped GaN layer (317);

a GaN layer (319) formed above the second In-doped GaN layer (317); and

a second electrode contact layer (320) formed above the GaN layer (319).

Nagahama does not teach that the first electrode contact layer (311) is formed above the super lattice structure layer (313).

However, Yamada, drawn to group III-nitride light emitting diodes (LEDs), teaches, from fig. 1, a contact layer (111) above a super lattice cladding layer (105).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Nagahama including a super lattice structure underneath the first contact layer as described by Yamada because it is well known in the art that a super lattice structure (alternating layers of two different several nanometer thick semiconductor materials) encourages better crystal growth of any layers grown thereon, thereby achieving better overall performance and efficiency. Edmond, column 15, lines 1-15 of US Patent No. 6,906,352, is cited for this well known position.

Nagahama also does not teach that the super lattice structure (313) is specifically a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer.

However, Emerson, drawn to group III-nitride light emitting diodes (LEDs), teaches, from fig. 1, a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer (16) beneath the active region (18). (See column 7, lines 19-22.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Nagahama including the super lattice structure of Emerson having alternating layers of $In_xGa_{1-x}N/In_yGa_{1-y}N$ instead of alternating layers of $Al_xGa_{1-x}N/GaN$ (as used by Nagahama) because either of these structures perform the same function of decreasing crystal defects in any group III-nitride grown thereon, thereby increasing device performance. Edmond, column 15, lines 1-15 of US Patent No. 6,906,352, is cited for this well known position.

Furthermore, examiner takes the position that the material selected for the super lattice structure, in view of those used in the prior art, is non-critical to the applicant's invention. Nagahama (with Yamada) discloses all the limitations of the claimed invention except for specifically teaching that the super lattice structure layer is, "an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer." It would have been obvious to one of ordinary skill in the art, at the time of invention, to replace the $Al_xGa_{1-x}N/GaN$ super lattice structure layer of Nagahama's device with one that is made of $In_xGa_{1-x}N/In_yGa_{1-y}N$ alternating layer (as disclosed above by Emerson), since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use (to enhance device crystal structure by reducing crystal defects) as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Note that Suzuki (US Patent No. 6,479,836), from column 11, lines 64-67 and Zheng (Non-patent document ref. [U]), from introduction, are cited for the non-criticality and well known use of this particular material structure.

Finally, Nagahama, Yamada, and Emerson do not specifically teach that the first electrode contact layer comprises a Si/In-codoped GaN layer.

Koike teaches, from fig. 2, a first electrode contact layer comprising a Si/In-codoped GaN layer (103). Layer 103 is an underlying layer which encompasses a GaN layer and silicon doped n-GaN (see column 11, lines 50-55). From column 16, lines 1-3, Koike teaches that this underlying layer may be doped with indium as well.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Emerson, and Yamada featuring a Si/In-codoped GaN electrode contact layer as described by Koike because indium doping in this underlying layer is done, "in order to improve crystallinity of the underlying layer. Improving crystallinity of the underlying layer results in further improving crystallinity of a layer growing thereon by lateral growth." (See column 16, lines 1-3.)

With respect to claim 5, Emerson teaches the active layer comprises a single or multiple quantum well structure. (See column 10, lines 62-65.)

2. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Yamada (US Patent No. 6,608,330), Emerson (US Patent No. 6,958,497), and Koike (US Patent No. 6,830,948) as applied to claim 1 above, and further in view of Lee (US Patent No. 6,720,570).

Nagahama, Emerson, Yamada, and Koike do not teach that the second electrode contact layer is an n-type electrode contact layer.

However, Lee, drawn to gallium nitride LEDs, does teach, from fig. 2, a second electrode contact layer (209) that is an n-type electrode contact layer. Additionally there is p-type layers, 205, 206, and 211, placed above the first n-type electrode.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Emerson, Yamada, and Koike utilizing the second n-type electrode contact layer of Lee because the first and second n-type electrodes with p-type layers between form an n-p-n arrangement which reduces the resistance of the device, thereby improving its efficiency. (See column 5, lines 1-9.)

With respect to claim 11, Nagahama, Emerson, Yamada, and Koike with Lee teach the device as stated above. Nagahama teaches that an n-type (first) electrode contact layer comprises a super lattice structure (see column 4, lines 24-29). Lee teaches that the second electrode contact is of n-type as stated above. Finally, Emerson teaches the specific use of $In_xGa_{1-x}N/In_yGa_{1-y}N$ as a super lattice structure as stated above.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Nagahama, Emerson, Yamada, and Koike with Lee having the second electrode contact layer comprising a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure for the obvious reasons stated above and also because the resistance of the device can be lowered thereby decreasing the voltage and current threshold of the device. (See column 4, lines 24-29 of Nagahama 6,849,864.)

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Yamada (US Patent No. 6,608,330), Emerson (US Patent No. 6,958,497), and Koike (US Patent No. 6,830,948) as applied to claim 1 above, and further in view of Tanizawa (US Patent No. 6,657,234).

Nagahama, Emerson, Yamada, and Koike do not specifically teach that the buffer layer comprises one selected from the group consisting of an InGaN/GaN super lattice structure, an $In_xGa_{1-x}N/GaN$ structure and an $Al_xIn_yGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ structure. Although Nagahama does teach, from column 3, lines 60-65, that, "it is preferable that at least one of the first and second buffer layers is a super lattice layer made by laminating nitride semiconductor layers of different constitutions."

Nevertheless, Tanizawa, drawn to nitride based semiconductor devices, does teach, from column 3, lines 56-62, a buffer layer comprises a superlattice structure that is formed by alternately stacking $In_zGa_{1-z}N/GaN$.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Emerson, Yamada, and Koike utilizing the $In_zGa_{1-z}N/GaN$ superlattice structure in the buffer layer because these are well known materials capable of functioning as a superlattice that increases the crystallinity of the buffer layer and layers grown thereon, thereby improving device performance. (See Edmond, column 15, lines 1-15 of US Patent No. 6,906,352)

Furthermore, examiner takes the position that the material selected for the super lattice structure in the buffer layer, in view of those used in the prior art, is non-critical to the applicant's invention. Nagahama (with Yamada and Emerson) discloses all the limitations of the

claimed invention except for specifically teaching that the buffer super lattice structure layer is, "an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer." It would have been obvious to one of ordinary skill in the art, at the time of invention, to have the buffer super lattice structure layer of Nagahama's device made of $In_xGa_{1-x}N/GaN$ (as disclosed above by Tanizawa), $Al_xIn_yGa_{1-x,y}N/In_xGa_{1-x}N/GaN$, or InGaN/GaN alternating layers, since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use (to enhance device crystal structure by reducing crystal defects) as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Note that Suzuki (US Patent No. 6,479,836), from column 11, lines 64-67 and Zheng (Non-patent document ref. [U]), from introduction, are cited for the non-criticality and well known use of this particular material structure.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Yamada (US Patent No. 6,608,330), Emerson (US Patent No. 6,958,497), and Koike (US Patent No. 6,830,948) as applied to claim 1 above, and further in view of Sverdlov (US Patent No. 6,266,355).

Nagahama, Emerson, Yamada, and Koike do not teach the device wherein the quantum well structure includes a low mole In-doped $In_xGa_{1-x}N$ layer, an $In_yGa_{1-y}N$ well layer and an $In_zGa_{1-z}N$ barrier layer.

However, Sverdlov, drawn to group III-V nitride based semiconductor devices, does teach a quantum well structure that includes a low mole In-doped (x=0.03-0.15) $In_xGa_{1-x}N$ layer (18), an $In_yGa_{1-y}N$ well layer (20) and an $In_zGa_{1-z}N$ barrier layer (22). (See column 4, lines 9-21)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Emerson, Yamada, and Koike utilizing the low mole In-doped $In_xGa_{1-x}N/In_yGa_{1-y}N$(well)/$In_zGa_{1-z}N$(barrier) layered structure because this arrangement can exclude the high temperature (900-1200°C) formation requirement of AlGaN layers thereby also avoiding crystal defects in the active region originating when heated at the higher formation temperatures. (See Background of the Invention columns 1 and 2.)

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Yamada (US Patent No. 6,608,330), Emerson (US Patent No. 6,958,497), Koike (US Patent No. 6,830,948), and Sverdlov (US Patent No. 6,266,355) as applied to claim 6 above, and further in view of Keller ("Growth and Properties of InGaN nanoscale islands on GaN").

With respect to claim 9, Nagahama, Yamada, Emerson, Koike, and Sverdlov teach the device as disclosed above.

Nagahama, Yamada, Emerson, Koike, and Sverdlov do not specifically teach that the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configuations.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Yamada, Emerson, Koike, and Sverdlov include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is

known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

With respect to claim 10, Nagahama, Yamada, Emerson, Koike, and Sverdlov teach the device as disclosed above.

Nagahama, Yamada, Emerson, Koike, and Sverdlov, do not specifically teach the device wherein the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration, and wherein the spiral surface configuration is extended to the surface of the $In_zGa_{1-z}N$ barrier layer.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configurations, and that the threaded dislocations can extend to layered surfaces formed thereon.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Yamada, Emerson, Koike, and Sverdlov include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

6. Claims 13, 15, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) in view of Koike (US Patent No. 6,830,948).

With respect to claim 13, Nagahama teaches, from fig. 9 (and columns 34-40), the nitride based 3-5 group compound semiconductor light emitting device comprising:

a substrate (301);

a buffer layer (304) formed above the substrate (301);

a first In doped GaN layer (312) formed above the buffer layer (304);

a first electrode contact layer (311) formed ***below*** the first In doped GaN layer (312);

an active layer (315) formed above the first electrode contact layer (311) and functioning to emit light;

a GaN layer (317 or GaN layer within superlattice 318) formed above the active layer (315); and

a second electrode contact layer (319) formed above the GaN layer (317).

Nagahama does not teach that a first electrode contact layer (311) is formed ***above*** the first In doped GaN layer (312). Also Nagahama does not specifically teach that the first electrode contact layer comprises a Si/In-codoped GaN layer.

However, Koike, drawn to group III-nitride light emitting diodes (LEDs), teaches, from fig. 7, underlying GaN layers (503) being doped with indium (see column 16, lines 1-5) and having a (n-type) contact layer (32) formed in and on (see fig. 1e) the In-doped GaN layer (31). Koike also teaches, from fig. 2, a first electrode contact layer comprising a Si/In-codoped GaN layer (103). Layer 103 is an underlying layer which encompasses a GaN layer and silicon doped n-GaN (see column 11, lines 50-55). From column 16, lines 1-3, Koike teaches that this underlying layer may be doped with indium as well.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Nagahama utilizing the arrangement whereby the first contact layer (311) would be above the first In doped GaN layer (312) as described by Koike because not

only does this result in the improved crystallinity of the GaN layers but also improves the crystallinity of any layer grown thereon, reducing defects in the device thereby resulting in better overall device efficiency and performance. (See column 16, lines 1-5.)

In addition, it would also have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama featuring a Si/In-codoped GaN electrode contact layer as described by Koike because indium doping in this underlying layer is done, "in order to improve crystallinity of the underlying layer. Improving crystallinity of the underlying layer results in further improving crystallinity of a layer growing thereon by lateral growth." (See column 16, lines 1-3.)

With respect to claim 15, Nagahama teaches from fig. 9, the device further comprising a second In-doped GaN layer (317) formed between the active layer (315) and the GaN layer (GaN layer within superlattice 318) and is p-type (i.e. doped with Mg).

With respect to claim 20, Koike teaches the device wherein the active layer comprises a single or multiple quantum well structure. (See column 10, lines 33-35.)

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) and Koike (US Patent No. 6,830,948), as applied to claim 13 above, and further in view of Lee (US Patent No. 6,720,570).

Nagahama and Koike do not teach that the second electrode contact layer is an n-type electrode contact layer.

However, Lee, drawn to gallium nitride LEDs, does teach, from fig. 2, a second electrode contact layer (209) that is an n-type electrode contact layer. Additionally there is p-type layers, 205, 206, and 211, placed above the first n-type electrode.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama and Koike utilizing the second n-type electrode contact layer of Lee because the first and second n-type electrodes with p-type layers between form an n-p-n arrangement which reduces the resistance of the device, thereby improving its efficiency. (See column 5, lines 1-9.)

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) and Koike (US Patent No. 6,830,948), as applied to claim 13 above, and further in view of Emerson (US Patent No. 6,958,497).

Nagahama and Koike teach the device as stated above. Nagahama teaches that an n-type (first) electrode contact layer comprises a super lattice structure (see column 4, lines 24-29). Koike teaches the various layers of the device being doped with indium.

Nagahama and Koike do not teach that the second electrode contact layer is specifically an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer.

However, Emerson, drawn to group III-nitride light emitting diodes (LEDs), teaches, from fig. 1, a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer (16) beneath the active region (18) utilized as an electrode contact layer. (See column 7, lines 19-22.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Nagahama, Koike, and Lee having the second

electrode contact layer comprising Emerson's $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure since this is a known material capable of forming a super lattice structure and also because the resistance of the device can be lowered thereby decreasing the voltage and current threshold of the device. (See column 4, lines 24-29 of Nagahama 6,849,864.)

Furthermore, examiner takes the position that the material selected for the super lattice structure, in view of those used in the prior art, is non-critical to the applicant's invention. Nagahama (with Koike and Lee) discloses all the limitations of the claimed invention except for specifically teaching that the super lattice structure layer is, "an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer." It would have been obvious to one of ordinary skill in the art, at the time of invention, to replace the $Al_xGa_{1-x}N/GaN$ super lattice structure layer of Nagahama, Koike, and Lee's device with one that is made of $In_xGa_{1-x}N/In_yGa_{1-y}N$ alternating layer (as disclosed above by Emerson), since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use (to enhance device crystal structure by reducing crystal defects) as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Note that Suzuki (US Patent No. 6,479,836), from column 11, lines 64-67 and Zheng (Non-patent document ref. [U]), from introduction, are cited for the non-criticality and well known use of this particular material structure.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) and Koike (US Patent No. 6,830,948), as applied to claim 13 above, and further in view of Tanizawa (US Patent No. 6,657,234).

Nagahama and Koike do not specifically teach that the buffer layer comprises one selected from the group consisting of an InGaN/GaN super lattice structure, an $In_xGa_{1-x}N/GaN$ structure and an $Al_xIn_yGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ structure. Although Nagahama does teach, from column 3, lines 60-65, that, "it is it is preferable that at least one of the first and second buffer layers is a super lattice layer made by laminating nitride semiconductor layers of different constitutions."

Nevertheless, Tanizawa, drawn to nitride based semiconductor devices, does teach, from column 3, lines 56-62, a buffer layer comprises a superlattice structure that is formed by alternately stacking $In_zGa_{1-z}N/GaN$.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama and Koike utilizing the $In_zGa_{1-z}N/GaN$ superlattice structure in the buffer layer because these are well known materials capable of functioning as a superlattice that increases the crystallinity of the buffer layer and layers grown thereon, thereby improving device performance. (See Edmond, column 15, lines 1-15 of US Patent No. 6,906,352)

Furthermore, examiner takes the position that the material selected for the super lattice structure in the buffer layer, in view of those used in the prior art, is non-critical to the applicant's invention. Nagahama (with Koike) discloses all the limitations of the claimed invention except for specifically teaching that the buffer super lattice structure layer is, "an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer." It would have been obvious to one of ordinary skill in the art, at the time of invention, to have the buffer super lattice structure layer of Nagahama's device made of $In_xGa_{1-x}N/GaN$ (as disclosed above by Tanizawa), $Al_xIn_yGa_{1-}$

$_{x,y}N/In_xGa_{1-x}N/GaN$, or InGaN/GaN alternating layers, since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use (to enhance device crystal structure by reducing crystal defects) as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Note that Suzuki (US Patent No. 6,479,836), from column 11, lines 64-67 and Zheng (Non-patent document ref. [U]), from introduction, are cited for the non-criticality and well known use of this particular material structure.

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) and Koike (US Patent No. 6,830,948), as applied to claim 13 above, and further in view of Sverdlov (US Patent No. 6,266,355).

Nagahama and Koike do not teach the device wherein the quantum well structure includes a low mole In-doped $In_xGa_{1-x}N$ layer, an $In_yGa_{1-y}N$ well layer and an $In_zGa_{1-z}N$ barrier layer.

However, Sverdlov, drawn to group III-V nitride based semiconductor devices, does teach a quantum well structure that includes a low mole In-doped (x=0.03-0.15) $In_xGa_{1-x}N$ layer (18), an $In_yGa_{1-y}N$ well layer (20) and an $In_zGa_{1-z}N$ barrier layer (22). (See column 4, lines 9-21)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Emerson, and Yamada utilizing the low mole In-doped $In_xGa_{1-x}N/In_yGa_{1-y}N$(well)/$In_zGa_{1-z}N$(barrier) layered structure because this arrangement can exclude the high temperature (900-1200°C) formation requirement of AlGaN layers thereby also avoiding crystal defects in the active region originating when heated at the higher formation

temperatures. (See Background of the Invention columns 1 and 2.)

11. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Koike (US Patent No. 6,830,948), and Sverdlov (US Patent No. 6,266,355) as applied to claim 21 above, and further in view of Keller ("Growth and Properties of InGaN nanoscale islands on GaN").

With respect to claim 24, Nagahama, Koike, and Sverdlov teach the device as disclosed above.

Nagahama, Koike, and Sverdlov do not specifically teach that the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configuations.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Koike, and Sverdlov include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

With respect to claim 25, Nagahama, Koike, and Sverdlov teach the device as disclosed above.

Nagahama, Koike, and Sverdlov, do not specifically teach the device wherein the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration, and wherein the spiral surface configuration is extended to the surface of the $In_zGa_{1-z}N$ barrier layer.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configurations, and that the threaded dislocations can extend to layered surfaces formed thereon.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Koike, and Sverdlov include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

12. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864) in view of Sverdlov (US Patent No. 6,266,355) and Koike (US Patent No. 6,830,948).

With respect to claim 34, Nagahama teaches, from fig. 9 (and columns 34-40), the nitride based 3-5 group compound semiconductor light emitting device comprising:

a substrate (301);

a buffer layer (304) formed above the substrate (301);

a first electrode contact layer (311) formed above the GaN buffer layer (304);

an active layer (315) formed above the first electrode contact layer (311),

a GaN layer (317) formed above the active layer (315); and

a second electrode contact layer (319) formed above the GaN layer (317).

Nagahama does not teach the device wherein the quantum well structure includes a low mole In-doped $In_xGa_{1-x}N$ layer, an $In_yGa_{1-y}N$ well layer and an $In_zGa_{1-z}N$ barrier layer.

However, Sverdlov, drawn to group III-V nitride based semiconductor devices, does teach a quantum well structure that includes a low mole In-doped (x=0.03-0.15) $In_xGa_{1-x}N$ layer (18), an $In_yGa_{1-y}N$ well layer (20) and an $In_zGa_{1-z}N$ barrier layer (22). (See column 4, lines 9-21)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama utilizing the low mole In-doped $In_xGa_{1-x}N/In_yGa_{1-y}N$(well)/$In_zGa_{1-z}N$(barrier) layered structure of Sverdlov because this arrangement can exclude the high temperature (900-1200°C) formation requirement of AlGaN layers thereby also avoiding crystal defects in the active region originating when heated at the higher formation temperatures. (See Background of the Invention columns 1 and 2.)

Also Nagahama does not specifically teach that the first electrode contact layer comprises a Si/In-codoped GaN layer.

However, Koike teaches, from fig. 2 and fig. 9, a first electrode contact layer comprising a Si/In-codoped GaN layer (103). Layer 103 is an underlying layer which encompasses a GaN layer and silicon doped n-GaN (see column 11, lines 50-55). From column 16, lines 1-3, Koike teaches that this underlying layer may be doped with indium as well.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama featuring a Si/In-codoped GaN electrode contact layer as described by Koike because indium doping in this underlying layer is done, "in order to

improve crystallinity of the underlying layer. Improving crystallinity of the underlying layer results in further improving crystallinity of a layer growing thereon by lateral growth." (See column 16, lines 1-3.)

13. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Sverdlov (US Patent No. 6,266,355) and Koike (US Patent No. 6,830,948) as applied to claim 34 above, and further in view of Keller ("Growth and Properties of InGaN nanoscale islands on GaN").

With respect to claim 38, Nagahama, Sverdlov, and Koike teach the device as disclosed above.

Nagahama, Sverdlov, and Koike do not specifically teach that the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configuations.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Sverdlov, and Koike include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

With respect to claim 39, Nagahama, Sverdlov, and Koike teach the device as disclosed above.

Nagahama, Sverdlov, and Koike do not specifically teach the device wherein the low mole In-doped $In_xGa_{1-x}N$ layer has a spiral surface configuration, and wherein the spiral surface configuration is extended to the surface of the $In_zGa_{1-z}N$ barrier layer.

However, Keller, drawn to the study of InGaN crystal growth, teaches, from the experimental procedure (2.) and results (3.), InGaN layers that are grown in a spiral mode, having spiral surface configurations, and that the threaded dislocations can extend to layered surfaces formed thereon.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device according to Nagahama, Sverdlov, and Koike include the In-doped $In_xGa_{1-x}N$ to be grown in spiral mode as described by Keller, since this is known to enhance the luminescence efficiency and increase radiative recombination lifetime. (See introduction (1.) and conclusion (4.))

14. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahama (US Patent No. 6,849,864), Sverdlov (US Patent No. 6,266,355) and Koike (US Patent No. 6,830,948)8 as applied to claim 34 above, and further in view of Lee (US Patent No. 6,720,570).

Nagahama, Sverdlov, and Koike do not teach that the second electrode contact layer is an n-type electrode contact layer.

However, Lee, drawn to gallium nitride LEDs, does teach, from fig. 2, a second electrode contact layer (209) that is an n-type electrode contact layer. Additionally there is p-type layers, 205, 206, and 211, placed above the first n-type electrode.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Nagahama, Sverdlov, and Koike utilizing the second n-type electrode contact layer of Lee because the first and second n-type electrodes with p-type layers between form an n-p-n arrangement which reduces the resistance of the device, thereby improving its efficiency. (See column 5, lines 1-9.)

Allowable Subject Matter

15. Claims 7, 8, 12, 16, 17, 22, 23, 36, and 37 are allowed.

16. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 7, 22, and 36, all claims containing similar subject matter, the prior record of art fails to teach or suggest a three layered quantum well active layer structure - low mole In-doped $In_xGa_{1-x}N$ layer/ $In_yGa_{1-y}N$ well layer / $In_zGa_{1-z}N$ barrier layer – wherein the low mole In-doped $In_xGa_{1-x}N$ layer has an In content smaller than that of the $In_zGa_{1-z}N$ barrier layer.

With respect to claims 8, 23, and 37, all claims containing similar subject matter, the prior record of art fails to teach or suggest a three layered quantum well active layer structure - low mole In-doped $In_xGa_{1-x}N$ layer/ $In_yGa_{1-y}N$ well layer / $In_zGa_{1-z}N$ barrier layer – wherein the low mole In-doped $In_xGa_{1-x}N$ layer, the $In_yGa_{1-y}N$ well layer and the $In_zGa_{1-z}N$ barrier layer have an In content expressed as $0<x<0.05$, $0<y<0.3$ and $0<z<0.1$, respectively.

With respect to claim 12, the prior record of art fails to show a buffer layer formed above the substrate; a first In doped GaN layer formed above the buffer layer; a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer formed above the first In-doped GaN layer; and a first electrode contact layer formed above the $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer; *wherein the first In-doped GaN layer and the $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer formed thereon are repeatedly layered in plurality.* [emphasis added]

With respect to claim 16, the prior record of art fails to teach or suggest a first electrode contact layer above a first In-doped GaN wherein a $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure layer is also formed between the first In-doped GaN layer and the first electrode contact layer.

With respect to claim 17, the prior record of art fails to teach or suggest a first electrode contact layer above a first In-doped GaN wherein an $In_xGa_{1-x}N/In_yGa_{1-y}N$ super lattice structure and an undoped GaN layer is formed between the first In-doped GaN layer and the first electrode contact layer.

Response to Arguments

17. Applicant's arguments filed on April 13th, 2006 have been fully considered but they are not persuasive.

The Applicant makes two basic arguments in response to the rejections made by the Examiner:

> **(a.)** That is, although Koike may teach that indium may be doped as an alternative, nowhere does Koike teach or suggest a Si/In codoped layer, as is posited by the Examiner. The other applied art references fail to address this deficiency of Koike. As a result, one of ordinary skill in the art would not be motivated by any combination of the applied art references to produce the invention of claims 1, 13, 27 or 34, which recite a Si/In codoped layer. A prima facie case of obviousness has thus not been made. Claims depending upon claims 1, 13, 27 or 34 are patentable for at least the above reasons.

> **(b.)** Further, the Examiner combines and recombines the applied art references to generate thirteen rejections. This plethora of rejections can only be achieved by impermissible hindsight reconstruction.

In reference to Applicant's argument **a**, the following passages from Koike (US Patent No. 6,830,948) are cited by the Applicant:

> **[passage 1]** However, Koike at column 11, lines 50-55 states: Notably, in formation of the GaN layer 32, silane (SiH4) was introduced so as to form a silicon (Si)-doped n-type GaN layer serving as the GaN layer 33. For the sake of simplified illustration, the drawing merely illustrates a GaN layer 103 including the mask 4 to inclusively represent the GaN layer 31 and the GaN layer 32.
>
> **[passage 2]** Further, Koike at column 16, lines 1-3 states: "***Alternatively***, indium (In) may be doped in the underlying layer ***in all the embodiments*** in order to improve crystallinity of the underlying layer." [emphasis added by Examiner]

However, the Examiner fully disagrees with the conclusion that the Applicant has come to, specifically that indium (In) is used as an alternative to silicon (Si) for doping the underlying layer.

First of all, Applicant has taken column 16, lines 1-3 and the word "alternatively" out of context. Koike uses the word "alternatively" here so as to make the point that indium can be doped in the underlying layers in ***all the embodiments*** of the invention, and ***not just the tenth embodiment*** to which this passage is contained.

In support of this position, Applicant is made aware of the fact that nowhere in Koike et al. is it stated that indium is to be used in replace of silicon as an n-type dopant in the electrode layer 103, 603 (i.e. the function of silicon doping is to provide an n-type conductive contact for the electrode, see passage 1) or conversely, that silicon can be used in replace of indium as crystallinity improving dopant (i.e. the function of indium doping is to improve the crystallinity

of the doped layer and layers formed thereon, see passage 2). In other words, nowhere in Koike et al. is it taught or suggested that silicon and indium can be used interchangeably as dopants, since Koike clearly uses the two dopants for different functions.

Second, Koike et al. does, in fact, teach that silicon and indium are to be doped in a single electrode layer. In support of this position, Applicant is referred to column 2, lines 55-60 of Koike et al. which states:

> **[passage 3]** In the present specification, the term "underlying layer" is used so as to collectively encompass a Group III nitride compound semiconductor single layer and a multi-component layer containing at least one Group III nitride compound semiconductor layer.

So after reading passage 3 and passage 1 and looking at figs. 1A-2, one comes to the clear and obvious conclusion that Koike encompasses layer 2 (single layer, 102 in fig. 2), and 31 and 32 (multi-component layer, 103 in fig. 2) as the underlying layer. Also, it is clear from passage 1 that layer 32 is doped with silicon. Finally, passage 2, states, undeniably, that the underlying layer (encompassing 2, 31, and 32 in figs. 1A-E and 102 and 103 in fig. 2) may be doped with indium. Therefore layer 32 (or 103 in fig. 2), which is doped with silicon to provide an n-type contact may also be, according to passage 2, also doped with indium to improve the "crystallinity" of the layer 32 (or 103 in fig. 2). Thus a prima facie case of obviousness exists.

In response to Applicant's argument **b**, that the number of references used by the Examiner to make the multiple rejections inherently requires hindsight reconstruction, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include

knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Applicant is also reminded that all the motivations used by the Examiner, in the 35 U.S.C. 103(a) rejections were supplied from the prior art made of record and were not simply the Examiner's creations or motivations.

Furthermore, in response to Applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Simply stated, no weight will be given to arguments that do not specifically point out any supposed errors in the rejections made by the Examiner.

The 35 U.S.C. 112 2nd paragraph rejections of claims 12 and 15 as well as the objection to claim 34 has been withdrawn in light of the appropriate amendments to these claims. The Applicant is thanked for cooperation on these matters.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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6/27/06

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